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Published in:
2023 IEEE Vehicle Power and Propulsion Conference, VPPC 2023 - Proceedings

DOI:
10.1109/VPPC60535.2023.10403368

Publication date:
2023

Document Version:
Accepted author manuscript

A 48V/360A Power Module-Based Paralleled-GaN Devices for Low-Voltage and High-Current Traction Inverter Applications

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Abstract—**Gallium nitride GaN power semiconductors are gaining popularity in high-power traction inverter applications. The phase current can reach up to several hundred amps in such cases. Therefore, paralleling multiple GaN HEMT transistors is undoubtedly a solution for increasing power capability and reducing conduction losses. This paper proposes a highly integrated paralleled GANs power module design (100V/360 A) based on an insulated metal substrate (IMS). The proposed design provides a low and symmetrical commutation loop inductance, high thermal conductivity, and a cost-effective solution. The double pulse test (DPT) experiment is successfully implemented at 48V/325A to validate the effectiveness of the proposed design.**

Keywords—GaN HEMT, Power module, packaging, high-current, paralleling.

I. INTRODUCTION

Light electric vehicles (LEVs) with low-voltage batteries of 48 V have gradually gained popularity in urban transportation environments due to their cost-effectiveness, safety, and convenience. Typically, the low-voltage and high-power traction inverter is capable of transferring power ranging from 5kW to 12 kW, with switching voltages ranging from 48V to 72V and currents ranging in the hundreds of amps. Therefore, paralleling discrete power devices is an everlasting solution for achieving high-power electric mobility applications. Over many years, paralleling conventional Si Mosfets has been maturely implemented in a variety of applications [1]. In comparison to Si devices, emerging wide bandgap (WBG) semiconductors, particularly Gallium Nitride (GaN) high electron mobility transistors (HEMTs), have ultra-fast switching frequency, lower on-state resistance, zero reverse recovery current, chip size reduction, and higher temperature operation [1]-[4]. Moreover, the characteristics of GaN HEMTs have been considered suitable for paralleling applications thanks to:

- Stable gate voltage threshold $V_{g(th)}$ over a wide temperature range *(T_j)*.
- Positive temperature coefficient and strong temperature dependency of $R_{DS(on)}$

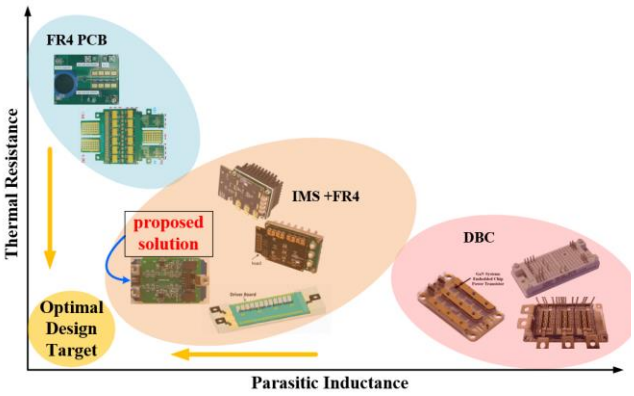


Fig. 1. The performance of packaging methods for GaN power modules.

However, the diverse parasitic effects become more severe in packaging paralleled multiple GANs due to high *di/dt* and *dV/dt* during switching transients. The asymmetrical PCB layout in the power loop and driving loop may lead to dynamically unbalanced current-sharing capability, especially in hard switching conditions at a high current of over 300A. In addition, gate voltage for driving GANs is more sensitive to parasitic inductance and parasitic capacitance in gate loop layout. The gate voltage breakdown of Si/SiC devices is typically around 20 V, and the voltage threshold Vgs(th) is 3 V, whereas GaN devices allow only 7 V and 1.4 V, respectively. As a result, there is a high possibility of being falsely triggered during the switching transient if the gate driver loop is not laid out properly. Furthermore, generating power losses are concentrated in compact-size GaN devices, which requires a proper thermal management solution. The packaging approaches of parallel-GAN power modules can be divided into three categories, as illustrated in Fig. 1. The first category is that the GAN dies are attached by direct-bonded copper (DBC) substrate and interconnected by the wire bond. DBC substrate typically

consists of a top layer of copper, a middle layer of ceramic for isolation, and a bottom layer of aluminum oxide (Al2O3) or aluminum nitride (AIN) for heat dissipation. Thus, high thermal and mechanical stresses can be sustained and are preferred for high-power applications ranging up to a few hundred kW. However, very little design flexibility is available for obtaining low and equal parasitic inductance in the power loop, resulting in poor switching performance [2], [3]. The second packaging method is to use a multi-layer PCB to have more freedom on the PCB [4], [5]. Where magnetic flux-cancelling designs can be effectively implemented on multi-layer PCB. The third design option for a high-current power module is to use an insulated metal substrate (IMS) [6],[7]. Which has a higher thermal resistance than DBC but a much lower thermal resistance than PCB. IMS board structure consists of a copper layer, a dielectric layer, and a thick aluminum/copper base for heat dissipation. The IMS thermal conductivity ranges from 2 to 7 W/mK depending on the metal base material and the dielectric thermal properties of the dielectric material. Cu-based IMS typically has better thermal conductivity than Al-based IMS. This paper aims to provide an effective solution for designing a high-power density GaN power module. The proposed design approach can be applied for paralleling both low-voltage (100V) and high-voltage (650V) bottom-cooled dies to fully utilize the device's capability. This study uses the sandwich configuration consisting of a single-layer IMS board with parallelized multiple GaN chips, decoupling capacitor boards, and a gate driver FR4 PCB to form a 100V/360A half-bridge power module. The advantages of the proposed paralleled GaN power module can be summarized as follows:

1) Symmetrical power commutation loop and gate loop. Therefore, even parasitic inductance can be achieved by equally distributed decoupling capacitors.
2) Excellent thermal conductivity IMS design allows for greater power loss dissipation while maintaining low parasitic inductances.
3) Low-cost and simple packaging solution while maintaining a robust switching performance with a small V_{DS} overshoot value and no ringing V_{GS} waveform under a very high switching current of a few hundred amps.
4) Partial DC-link capacitors can be assembled directly on the power module without sacrificing power density.
5) The proposed power module has the same outer configuration as the standard commercial power modules, making it suitable for a wide range of high-power traction inverter applications.

II. DESIGN CONSIDERATION FOR THE PROPOSED GAN MODULE

A. Design Procedure

For a high-power module packaging design, switching performance and heat dissipation capability are the most important factors to ensure a reliable operation under high electrical and thermal stress. Due to the high complexity of multi-physics fields, mathematical model expressions described by enormous high-order differential equations become infeasible. Therefore, the design approach using electrothermal finite element analysis (FEA) software frameworks is employed to shorten development time and fabrication costs by reducing the number of hardware prototypes that must be built. As depicted in Fig. 2 of the design procedure, the software design framework starts with different paralleled-GaNs PCB layout solutions using Altium Designer. The PCB layout from Altium Designer is exported to an open database exchange data (ODB) format file, namely ODB++, which is then imported into Ansys SIwave for geometry, layer, and material reconfiguration. Afterward, parasitic inductances of the power loop are computed by Ansys Q3D.

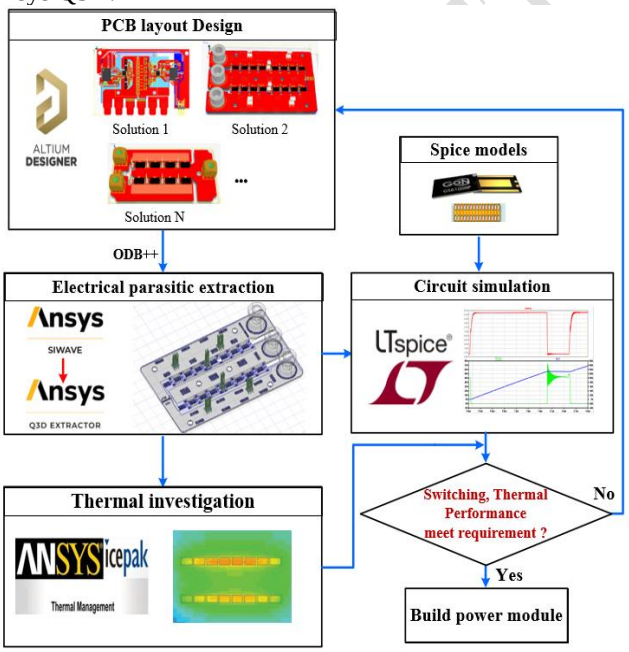


Fig. 2. Design framework and procedure of the proposed power module prototype.

To verify the switching performance, the circuit simulation model of the double pulse test (DPT) setup is created by LTspice software. Spice models of GaN devices provided by manufacturers and extracted parasitic elements from Ansys Q3D are used as input simulation parameters. The potential failure of the power module due to high parasitic inductance and asymmetrical PCB layout can be predicted throughout the switching waveforms of V_{DS} and V_{GS} of the half-bridge module. Following this step, the power module's thermal behavior can also be estimated by the Ansys Icepak sub-simulation tool. Finally, the best design solution is selected if it meets all switching and thermal requirements.

B. Power module structure and layout considerations

Low and symmetrical power loop inductance and high thermal conductivity are critical factors in high-power module design. Hence, the optimal layout and packaging structure need to be thoughtfully considered. Fig. 3 shows the circuit diagram with existing parasitic inductances of the proposed design. Fig. 4 (a) shows the exposed 3-D model view, and (b) is the assembled 3-D model of the proposed half-bridge power. The proposed design selects the vertical power loop configuration and hybrid IMS PCB structure for achieving flux canceling and heat dissipation capability. Mounted to the single-layer IMS board are a total of eight GS6100P GaN chips to build a half-bridge power module. Unlike previous hybrid PCB structures, the proposed

structure has four decoupling capacitor boards, distributed equally to each pair of high-side and low-side GaN chips by +DC and -DC copper bars with a dimension of 40 mm× 5 mm × 0.8 mm.

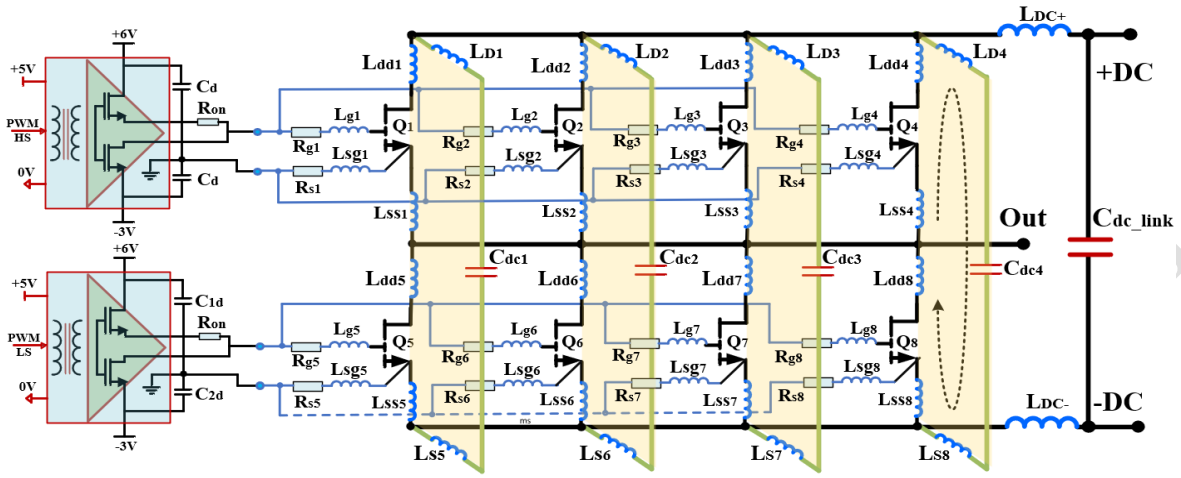


Fig. 3. Circuit diagram of the half-bridge with 4× GaN HEMTs in parallel with packaging parasitic inductances.

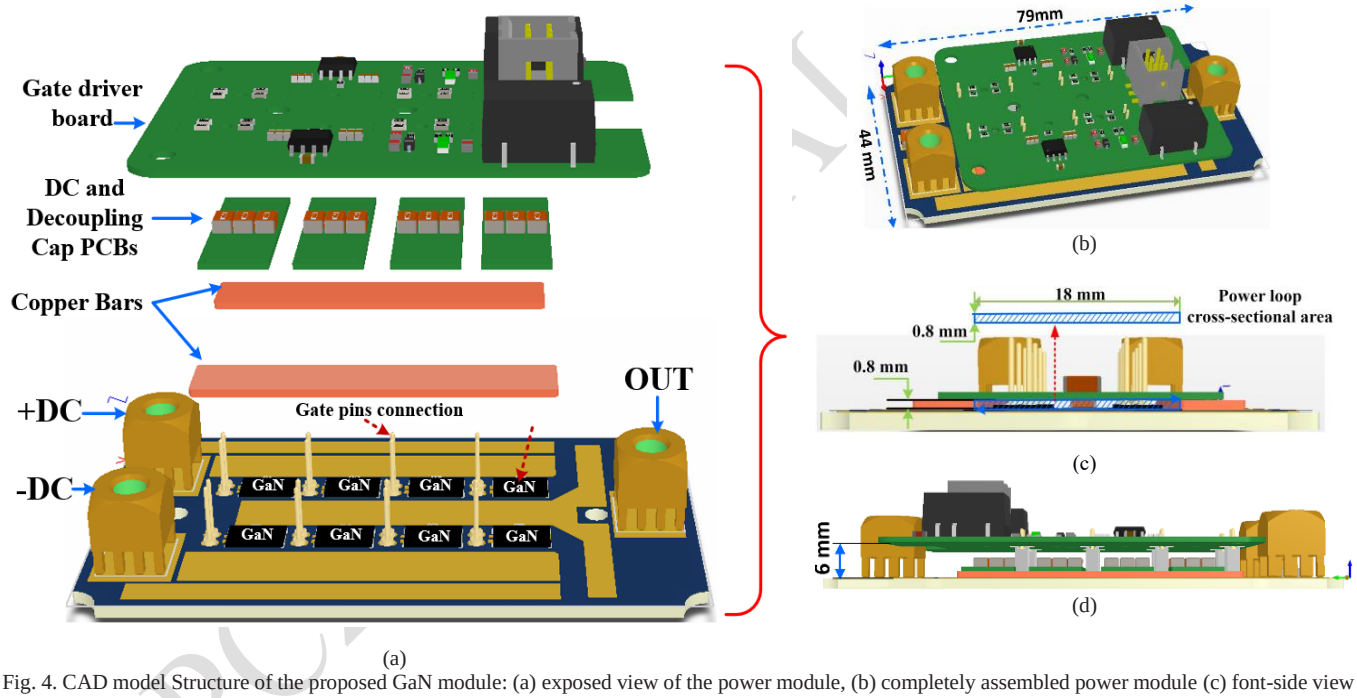


Fig. 4. CAD model Structure of the proposed GaN module: (a) exposed view of the power module, (b) completely assembled power module (c) font-side view of the power module, (d) left-side view of the power module

TABLE 1. PROPERTIES AND PARAMETERS OF THE PROPOSED IMS STRUCTURE

IMS structure parameters	Materials	Values
Power board × 1	IMS	
○ Dimension		44×79 mm
○ Numbers of layers		Single layer
○ Conductive layer	Copper	3oz-105 µm
○ Metal base	Aluminium	2 mm
○ Insulator layer thickness	polymeric film	76 µm
○ Thermal conductivity		2 W/mK
Decouple Cap board × 4	FR4-PCB	
○ Dimension		20×8 mm
○ Numbers of layers		2-layers
○ Conductive layer	Copper	2 oz-70 mm
○ PCB thickness		0.8 mm
○ Top-side Capacitor	Cemanic-X7R	3×100 nF
	Cemanic-X7R	3×1µF

The use of copper bars to vertically connect the IMS board and decoupling capacitor PCBs reduces stray inductance compared to using vias, or multi-pin header strips in previous structures [4]. Thanks to the low-profile 0.8 mm copper bar and 0.8-mm two-layer capacitor PCBs, the cross-sectional commutation loop area can be minimized, as depicted in Fig. 4 (c). This structure also contributes to the high current carrying capability of the +DC and -DC terminals. Fig. 4 (d) shows the side view of the power module. The gate and source pins of each GaN device are connected to the gate driver board by 6 mm brass pins. Thus, the gate signals can be delivered equally to the switches without intersecting with any high-power and high di/dt path. Table 1 lists the design parameters of the proposed power board.

C. Power loop parasitic extraction

Power loop inductance has a significant impact on the overall switching performance of the proposed power module. Thus, it is extracted in this section using Ansys Q3D. As shown in Fig. 5, the 3D model with the copper layout of the power module is designed using Altium Design software and imported into the Ansys SIwave /Q3D simulation environment.

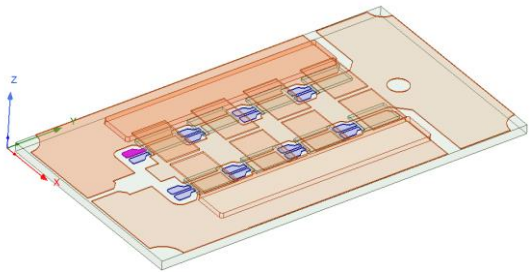


Fig. 5. Power-loop inductance simulation setup

After defining the material and geometry dimensions, the current direction of the power loop is assigned by sink/source nets configuration. Finally, the total power and gate loop inductances are obtained and listed in Table 2.

TABLE 2. PARASITIC INDUCTANCES EXTRACTION

Parameter	Symbol	Values
Power loop inductance	L_{Loop1} -L_{Loop4}	~1.4 nH
Quasi-common source inductance	L_{ss5} - L_{ss8}	< 0.05 nH
Gate loop inductance	L_{g_total}	~6.5 nH

The simulation results show a single power loop inductance of 1.4 nH. More notably, the use of thin copper bars allows for extremely low quasi-common source inductance (less than 0.05 nH).

D. Gate driver design considerations for paralleling GaNs

To drive multiple GaN devices, the single commercial gate driver IC Si2871 is selected due to its high pulse sink/source current rating (4A/4A) with fast transient during turn-on and turn-off times. Because of the very low turn-on threshold voltage (1.3V for GS61008P), the bipolar supply voltage is used for both high-side and low-side drivers to avoid the risk of false turn-on triggers due to miller effects. However, a large negative voltage V_{gs_off} causes significantly high voltage drop V_{SD} during deadtime period in reverse conducting mode as in (1).

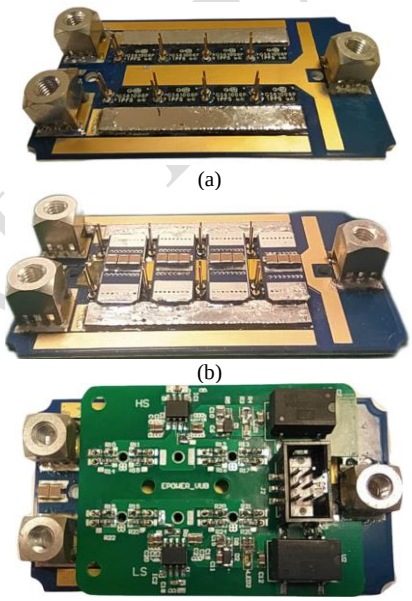
$$\begin{cases} V_{SD} = V_{th} - V_{gs\_off} + I_D \times R_{DS_{on}} \\ -V_{gs\_off\_max} \le V_{gs\_off} \le 0 \end{cases} \quad (1)$$

Moreover, it also increases the possibility of GaN destruction since V_{gs_off} excess the maximum negative value $V_{gs\_off\_max}$ of -10V (GS61008P). To prevent the gate-source voltage oscillations that lead to false turn-on of GaN devices, there are several techniques adopted in the proposed gate driver design, as follows:

1) Split output is recommended to be able to control individually both the turn-on and turn-off stew rate of GaNs. In addition, the low resistance in the turn-off loop reduces the adverse Miller effect.
2) Select the GaN chip with Kelvin source pin configuration and minimize the overlap between the switching node path and gate driving path to ensure the decoupling between the gate and the power loop.
3) Separate the gate driver board and power board to minimize the crosstalk due to high dv6 mm/dt and di/dt, through the parasitic capacitance and parasitic common source inductance.
4) The distributed decoupling capacitors in the proposed power board design significantly contribute to equalizing the common source parasitic inductances ($L_{S5}-L_{S8}$) resulting in a reduction of ringing gate-source voltage.
5) Even gate-driving loop inductances can be obtained due to the identical PCB layout of the gate driver board. In addition, split on and off resistors (R_{g1}- R_{g8}, R_{s1}- R_{s8}) of 2 Ω are placed at both gate and source of each GaN device to reduce the effects of circulating resonant current among gate driver loops [4].

III. POWER MODULE FABRICATION PROCESS

The fabrication flow for the proposed power module is depicted in Fig. 6 and can be described as follows:



(a)

(b)

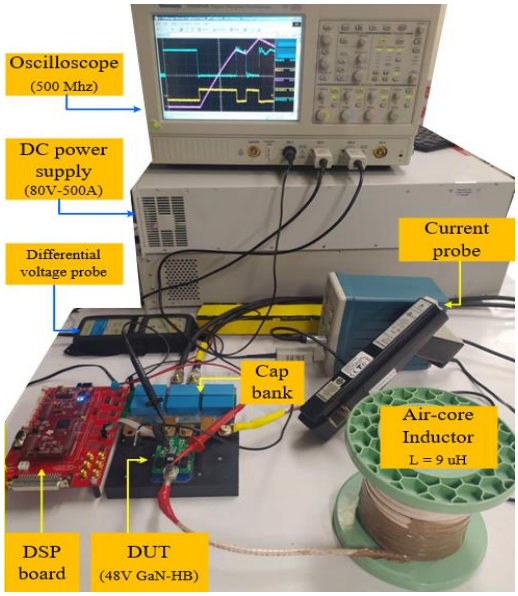
(c)

Fig. 6. Fabrication process of the half-bridge module: (a) step 1, (b) step 2, (c) step 3.

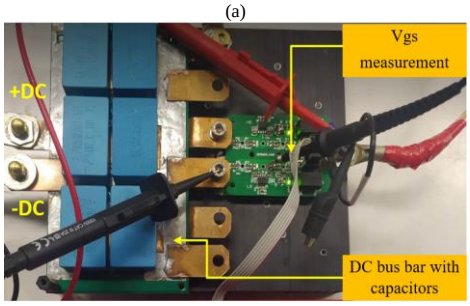
Step 1: The procedure starts with the application of the acronym for Sn/Ag/Cu alloy soldering paste (SAC) to a 3-oz IMS board with a 100-μm-thickness stencil sheet. Following that, eight discrete GAN dies are placed on the IMS board, and sixteen copper pins are used to connect the gate and source pins of each die for driving signals. Then, two 8 mm × 4 mm × 0.8 mm copper bars and +DC, -DC, and OUT terminals are put on the board as shown in Fig. 6(a). Lastly, the board is ready for the reflow soldering process.

Step 2: Decoupling and partial DC link capacitors are soldered on 2-layer FR4 PCBs with a copper thickness of 2 oz and a PCB thickness of 0.8 mm. Three 100nF/100V and three 1uF/100V DC link capacitors are soldered on the on the top side. Afterward, four capacitor PCBs are assembled on the IMS power board. Each capacitor PCB is placed on the +DC and -DC copper bars. Thus, each pair of the HS and LS-MOSFET has its own capacitor PCB. The second reflow soldering

process is applied for mounting the capacitor



(a)



(b)

Fig. 8. DPT test setup. (a) DPT hardware connection, (b) detailed power module connection zoomed in.

PCB on the main power module. The power IMS board has been completed after this step as in Fig. 6(b).

Step 3: The gate driver board with 1mm thickness is soldered by a conventional process. Lastly, the gate driver board is mounted to the IMS power board by 6mm gate-source brass pins. The completely assembled power module is shown in Fig. 6(c)

IV. Experimental Validation

In this article, the double pulse test DPT has been conducted to verify the switching and thermal performance of the proposed design. The capability of high current and thermal stress handling is evaluated by testing setup diagrams as shown in Fig. 7.

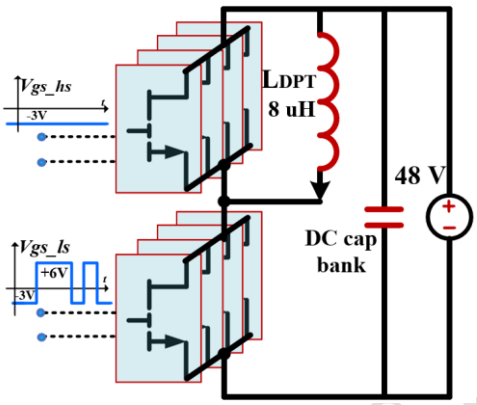
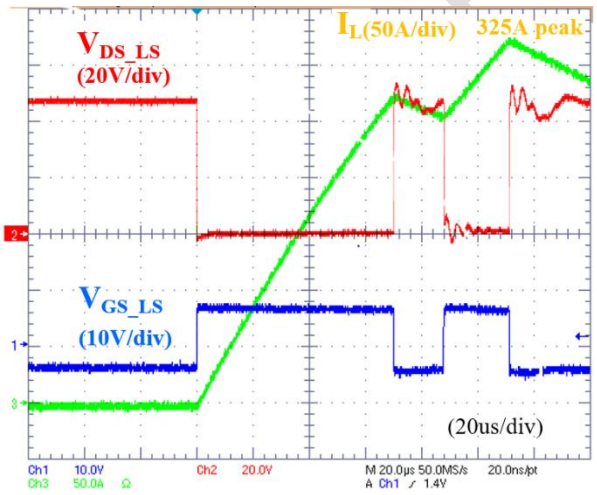
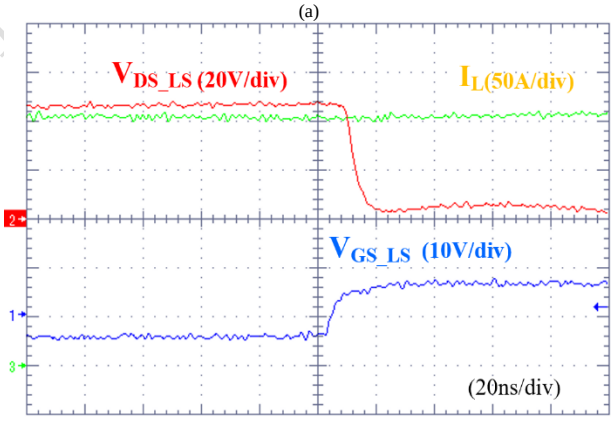


Fig. 7. Schematic of the experimental DPT setup



(a)



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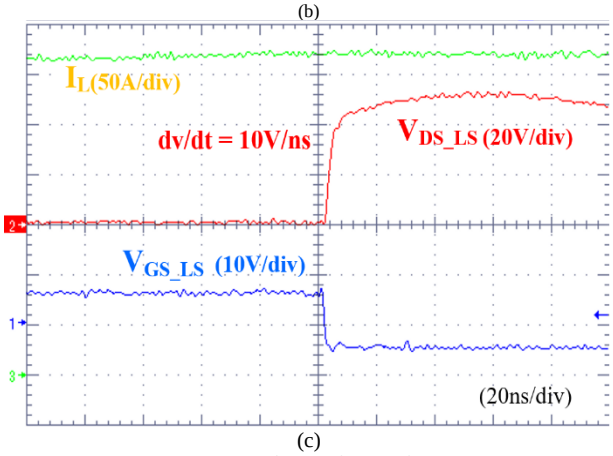

(c)

Fig. 9. Experimental DPT waveforms of the half-bridge module: (a) DPT waveform of the half-bridge power module, (b) detailed turn-on transient waveform, (c) detailed turn-off transient waveform.

A DPT setup is implemented by using an air core inductor of 8µH as the load and a 400µF DC link capacitor bank. The high-side paralleled GaN devices are operated in freewheeling mode by applying continuous -3V at the top-side gate driver. Meanwhile, low-side devices work as the main switch. The whole setup of the test platform is demonstrated in Fig. 8. The double pulse signal is provided by a programmed DSP launchpad TMS320F28379D board. The switching note voltage V_{DS} is measured by a 100 MHz differential probe (Tektronix P5205A). The V_{GS} waveform is captured by a high-bandwidth passive probe. A TCP0150A probe with the 500 A peak current capability is used to measure the high-current waveform of the output inductor. The measured waveforms are recorded by Tektronix 500Mhz TDS5054B oscilloscope. Fig. 9 shows experimental DPT waveforms, including V_{DS}, $V_{GS,}$ and I_{L_DPT}, respectively. The proposed power module has successfully switched at 48V/325A with an 8V overshoot voltage and *dV/dt* of 10V/ns. Fig. 9(b) and (c) show clean and stable turn-on and turn-off waveforms, which meet the requirements of traction inverter applications.

V. Conclusion

In this paper, a high-power GANs-based 360A/100V half-bridge module has been built using the proposed paralleling solution. This design concept demonstrates excellent performance in several aspects, including a low and even communication power loop among each paralleling pair of high-side and low-side GaN chips, good thermal conductivity, a reliable switching gate driver, low complexity, and cost reduction. The switching performance is successfully validated by the robust 48V-325A DPT experimental waveforms. Furthermore, this module can be packaged in the same terminal configuration as a standard commercial power module, making it suitable for a wide range of applications, particularly low-voltage and high-current traction inverters.

Acknowledgment

This research has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101006943, under the title of URBANIZED (https://urbanized.eu/). The authors also acknowledge Flanders Make for the support to our research group.

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