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A Differential GaN Power Amplifier with <1° AM-PM Distortion for 5G mm-wave Applications

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***Abstract*—This paper presents a 0.15µm GaN power amplifier (PA) for 5G applications. The differential two-stage PA contains a high-order interstage matching network for AM-PM distortion compensation without adding any extra active device. The implemented PA achieves a peak power added efficiency (PAEsat) of 25.5% and saturated output power (Psat) of 32.1dBm at 26GHz. The simulation and measurement results show less than 1 degree AM-PM variation up to Psat across a 24GHz to 30GHz frequency band.**

***Keywords*—AM-PM distortion, GaN, 5G, power amplifiers.**

I. Introduction

To fulfill the insatiable demand for high data-rates, millimeter-wave (mm-Wave) 5G communication standards use high-order, complex modulation schemes with high peak-to-average power ratios (PAPRs) and large RF bandwidths. This puts stringent linearity requirements on the PAs [1]. In various practical applications, digital predistortion (DPD) is applied to linearize the transmitter, yielding a higher PA efficiency and a lower ACPR. While AM-AM distortion compensation simply needs a static lookup table as a function of different input powers, AM-PM distortion compensation might need the implementation of a Volterra filter with deep memory, consuming much more power than AM-AM linearization. Consequently, minimizing AM-PM distortion is vital.

GaN HEMT devices enable the design of high-efficiency PAs with incomparable output power levels. However, GaN devices come with AM-AM and AM-PM distortion [2] that constrain the handling of modulated signals with a high PAPR. Therefore, not only efficiency maximization but also nonlinear behaviours, including AM-AM and AM-PM distortion, must be considered in the design process. Analog AM-PM predistortion has already been demonstrated in CMOS using varactor-based techniques. The designs in [3] and [4] improve the PA intrinsic linearity using PMOS-based AM-PM correction methods at sub-6GHz and mm-wave frequencies, respectively. Although such techniques considerably reduce the design overhead of external linearization approaches, the inclusion of an additional capacitive and lossy element to reduce AM-PM distortion degrades gain and efficiency, especially at mm-wave frequencies.

This paper presents AM-PM distortion compensation technique utilizing the intrinsic non-linear feature of the transistor in the differential PA. A high-order interstage matching network in between the two amplifying stages is proposed that not only fulfills the impedance matching but also reduces the AM-PM/AM-AM distortion in a broad frequency range. A Marchand balun (MB) together with extra matching elements are used for broadband input and output matching. The simulation and measurement results prove that the proposed topology reduces AM-PM distortion to less than 1 degree in a broad frequency range, which is the lowest AM-PM distortion among GaN PAs at a similar frequency band.

II. GaN-on-SiC Technology

The circuit is fabricated in a GaN-on-SiC technology with 0.15µm gate length on a 100-µm-thick substrate. For stable operation at high supply voltages up to 28V, this process uses a source-coupled field plate structure that is optimized for a high breakdown voltage. For the HEMT devices, the maximum cutoff frequency f_T is 35GHz while the maximum f_{MAX} is 80GHz. The process also offers air bridges, and back-via contacts, which not only provide a path to ground from the surface to the backside of the SiC substrate, but also play a critical role in heat transfer to an off-chip heat sink.

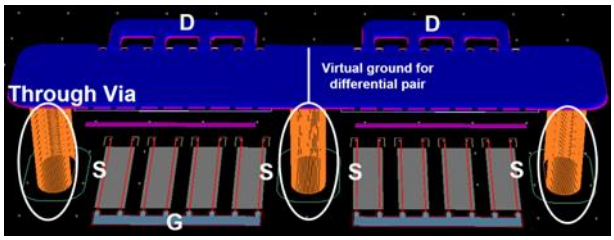


Fig. 1. Layout of a differential pair with grounded source node.

A. Transistor layout

The differential PA uses a differential pair with grounded source node(see Fig. 1). All transistors use multiple gate fingers and each finger width is 100µm. Transistors in the driver stage (=1st stage) and power stage (= 2nd stage) use 4 and 8 fingers, respectively. Due to the large size and the use of multiple fingers used for a high output power, the threshold voltage (Vth) for each finger might be different, which might corrupt the differential operation. To limit Vth fluctuations, through vias (TSV) are added as shown in Fig. 1. Measurements on the chip of the drain current of corresponding devices, referred back to the gate-source voltage shows that the input offset voltage of the output differential pair is less than 10mV, sufficiently guaranteeing the differential operation of the power core.

B. *Limitations on passive components*

The GaN technology has two gold metal layers available in the back-end-of-line. The lowest metal exhibits a sheet resistivity that is 5 times higher than the top metal. The maximum current density allowed for the low metal layer requires wider traces, causing larger parasitic for high-power and high-frequency PAs. This limits the use of the lower metal layer. Consequently, broadside coupler and transformers widely utilized in differential amplifier designs are limited in GaN process, which forces most of the GaN designs to be single-ended topologies.

C. *Choice of the supply voltage*

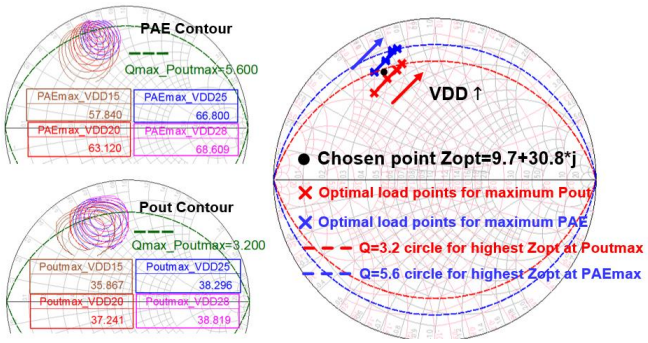


Fig. 2. Load pull simulations for differential end transistor at different VDD values: 15/20/25/28V.

The most important advantage of a GaN technology is the ability to operate with a high supply voltage for a large output power. The transistor breakdown voltage here is more than 120V, enabling a supply voltage up to 28V. Fig. 2 left shows the PAE and Pout loadpull contours for VDD ranging from 15V to 28V and Fig. 2 right extracts the optimal load points corresponding to maximum PAE/Pout at 1.5dB gain compression. For higher VDD values, the quality factor (Q) of the optimal load impedance (Zopt) increases and moves towards the edge of the Smith chart. Meanwhile, PAE and Psat do not improve significantly after 20V. As the high-Q matching degrades the bandwidth and passive efficiency, a VDD of 20V is chosen for this PA design.

III. Differential PA Design

A. *Architecture*

The proposed two-stage PA, see Fig. 3, utilizes a differential topology both for the driver (M1a, M1b) and power stage (M2a, M2b). At the input and output a balun is used. Compared to a single-ended PA, a differential one has a 3-dB greater output power and input and output impedances that are twice as large. This is particularly advantageous for high-power transistors that inevitably come with extremely low terminal impedances, which complicates impedance matching. Furthermore, as the performance of the high-power transistor can be easily degraded with an unwanted source degeneration by inductance and resistance on the ground to VDD return paths, it is desirable to use a differential design providing a local virtual ground. Due to the fact that there is only one metal layer available for the passive design as mentioned in Section II.B, this work uses a Marchand balun (MB) in the input and output matching together with the series capacitor for the DC blocking. Additional passive elements in the input and the output increase the order of the passive network and minimize the insertion loss at a large bandwidth. A high-order matching network is also applied in between the driver and the power stage for lowering the AM-AM/AM-PM distortion and the insertion loss in broad frequency range. RC filters are added at the gate of the transistors making the transistors unconditionally stable. The gates of corresponding transistors are biased separately to enable a DC offset compensation if needed.

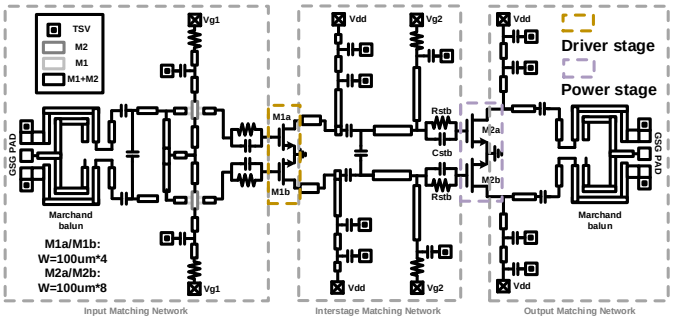


Fig. 3. Proposed PA architecture.

B. *AM-PM & AM-AM distortion compensation*

One of the AM-PM distortion compensation methods that does not require extra circuit elements and that is regularly used in CMOS technology, is to tune the gate bias of the amplifying transistors differently in the driver stage (DA) and the power stage (PA), as illustrated in Fig. 4 (a).

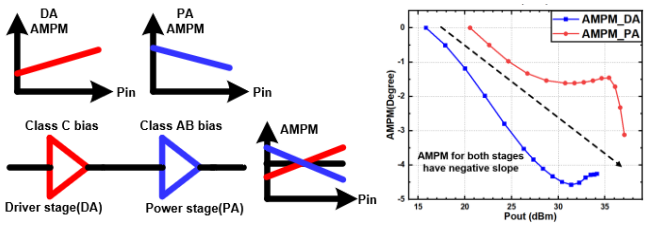


Fig. 4. (a)AM-PM distortion compensation by combining a class C (or deep class B) regime with a class AB regime for driver and power stage; (b) AM-PM distortion at 28GHz of the 2 stages at the selected optimum load.

This approach relies on AM-PM distortion from the DA, biased in class C or deep AB, that is opposite to the AM-PM distortion of the PA stage biased in class AB for more gain. However, class C operation reduces the gain at 28GHz significantly. Instead, class AB operation is chosen to provide sufficient gain and efficiency. As a result, both stages contribute to AM-PM distortion when Pin increases, as shown in Fig. 4 (b), yielding a poor linearity for modulated signals.

The two main factors that affect AM-PM distortion are the gate-drain parasitic capacitance Cgd and the gate-source parasitic capacitance Cgs [2,8]. Due to the field plate structure at the source side, Cgs is about 10 times larger than Cgd. For a high-power PA, the design bottleneck with respect to minimization of AM-PM distortion occurs at the interstage matching, since it not only connects the largest Cgs from the

power stage but also presents a non-linear impedance at the output of the driver stage. The mutual impact between the driver stage and the power stage due the nonlinear loading again complicates AM-PM distortion minimization. The interstage matching network (IMN) in this work is designed for multiple purposes: (1) AM-PM compensation; (2) AM-AM compensation; (3) low insertion loss; (4) broadband operation. With a first-order LC matching network, see Fig. 5 (a), the output resistance and capacitance of the driver stage and the input resistance and capacitance of the power stage change in same direction with increasing input power (Pin) resulting in a constructive AM-PM distortion.

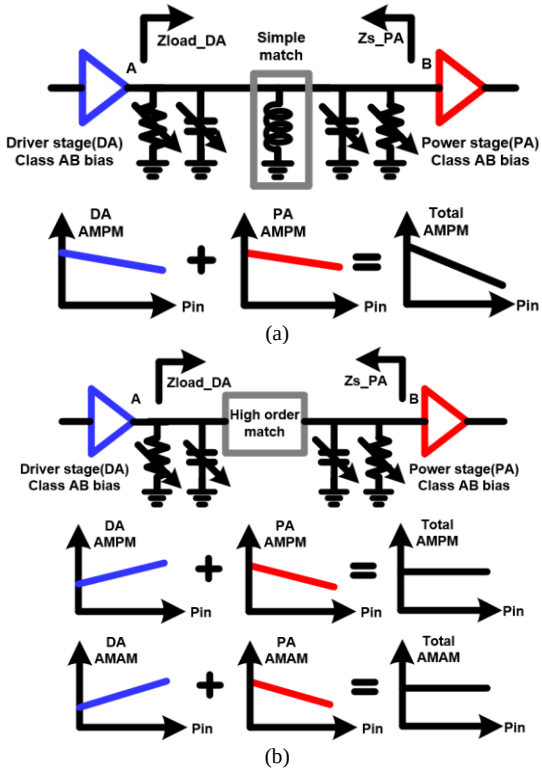


Fig. 5. AM-PM distortion (a) with a simple interstage matching network and (b) with the high-order interstage matching network shown in Fig.1.

Instead, this work uses a high-order passive network for the IMN, see Fig. 5(b). This transforms the output impedance of the driver stage (Zload_DA at point A) to compensate for the input impedance variation (impedance Zs_PA at point B) with increasing Pin. Likewise, the IMN compensates the impedance variation of Zload_DA with Zs_PA. The net effect is a low AM-PM distortion for both the driver and power stage. Further, the AM-AM distortion is reduced by making the contributions of the two stages opposite together with a slight tuning on the gate bias for the driver stage, which barely impacts the AM-PM flatness. To achieve a low AM-PM distortion over a broad frequency range with minimal insertion loss, it is also necessary to add a number of the passive components to have a more degree of freedom. The input and output matching network of the driver and power stage is also designed such that the miller effect from Cgd does not deteriorate AM-PM distortion.

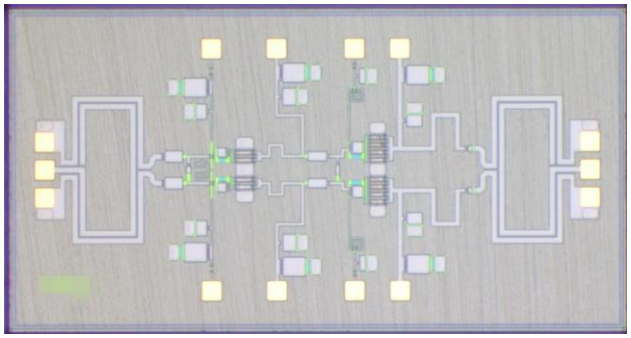


Fig. 6. Micrograph of the GaN PA. Chip size is 2.7x1.4mm^2.

IV. MEASUREMENT RESULTS

The differential PA is fabricated in 0.15μm GaN technology (see Fig.6) and tested with both continuous-wave (CW) and modulated signals. The measured small-signal S-parameters and the simulated values are shown in Fig.7: S21 remains above 10dB from 24GHz to 31GHz and corresponds well with simulations. The minimum of S22 has shifted to a lower frequency but with a wider bandwidth, which covers the desired frequency range.

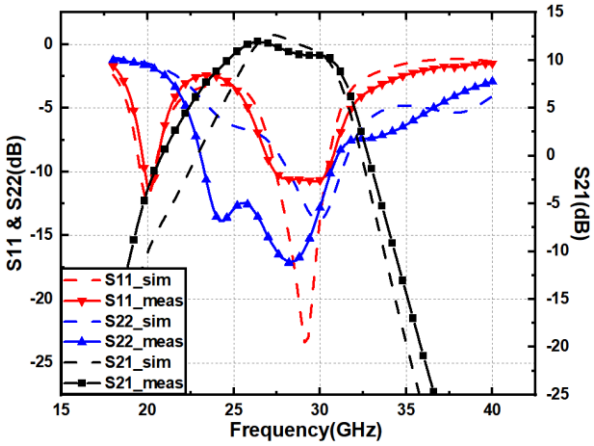
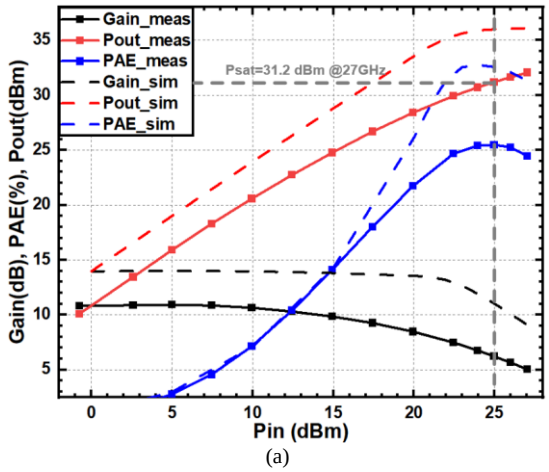
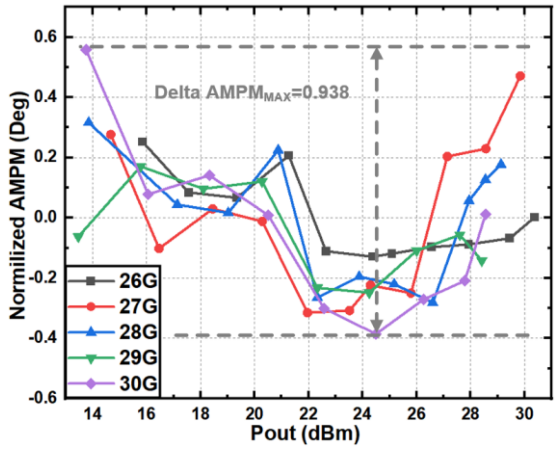


Fig. 7. S-parameter measurement results.



(a)



(b)

Fig. 8. Large-signal measurement results with a CW input at 27GHz: (a) Pout, PAE and Gain versus Pin; (b) normalized AM-PM distortion versus Pin.

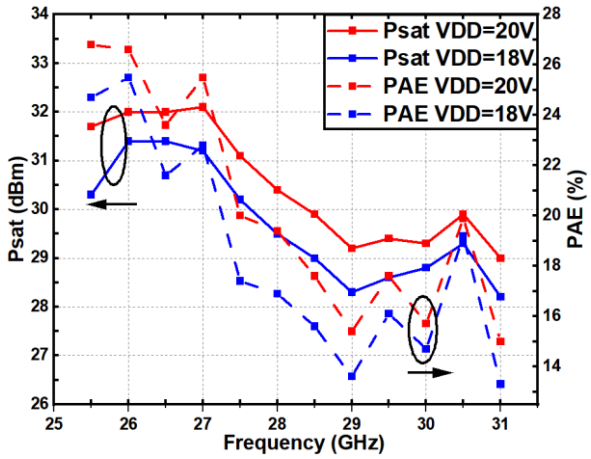


Fig. 9. Large CW signal measurement results: saturated power & PAE versus frequency.

Fig. 8 (a) shows the large-signal performance parameters Pout, PAE and Gain with AM-AM distortion at 27GHz. With a CW input signal, gain compression is more severe in measurements than in simulations. It is shown in [2] that the charge trapping in GaN devices leads to self-biasing, that can induce soft compression of an otherwise almost flat AM-AM gain plot. Together with thermal effects, that are not modelled, the saturated output power is 3.5dB less compared to simulated Psat. The saturated PAE is also limited since peak power is limited. However, the low AM-PM distortion as obtained in simulations is also observed in measurements: Fig. 8 (b) shows the measured AM-PM distortion at different frequencies between 26GHz and 30GHz. Over this frequency range the AM-PM variation is less than 1 degree, which agrees well with simulations.

Fig. 9 shows the saturated output power and corresponding PAE at different frequencies. The efficiency remains above 15% from 25GHz to 30.5GHz while the saturated output power remains above 29dBm with a supply voltage of 20V. With a supply voltage of 18V, the PA shows a slightly lower efficiency and output power. This proves the trade-off between output power and efficiency. A comparison to the state-of-the-art 5G PAs is shown in Table I. This work exhibits a high output power, comparable efficiency while achieving ultra-low AM-PM distortion over a broad frequency range. To the authors' best knowledge, this PA exhibits the lowest AM-PM distortion among the GaN PAs operating in a similar frequency range.

Table I. Performance comparison with the state-of-the-art 5G PAs.

Ref.	ISSCC 2018[4]	JSSC2018 [5]	IMS2020 [6]	TMTT2021 [7]	This work
Tech.	65nm CMOS	28nm CMOS	150nm GaAs	100nm GaN	150nm GaN
Freq. (GHz)	28	34	20-30	28-39	24-30
VDD (V)	1.1	0.9	5	15	20
Gain (dB)	15.8	20.8	23.4	20	11.9
Psat (dBm)	15.6	16.6	23	38.2	32.1
PAEmax (%)	41	24.2	19.5	26.1	26.8
AM-PM (Deg.)	<1	<1.1	NA.	NA	<1

V. Conclusions

A differential two-stage GaN PA for 5G mm-wave applications has been presented. The circuit uses Marchand baluns for input and output matching and a high-order matching network between the driver and power stage for AM-PM distortion compensation. Experimental results verify that the designed PA presents a high output power and efficiency while maintaining a flat AM-PM curve from 26GHz to 30GHz. The proposed AM-PM distortion compensation drastically simplifies predistortion, which reduces the transceiver design complexity.

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