

## Design and Implementation of a Digital Mixer with Digital Logic

Niyonkuru, Leonidas; Vandersteen, Gerd; Van Biesen, Leo

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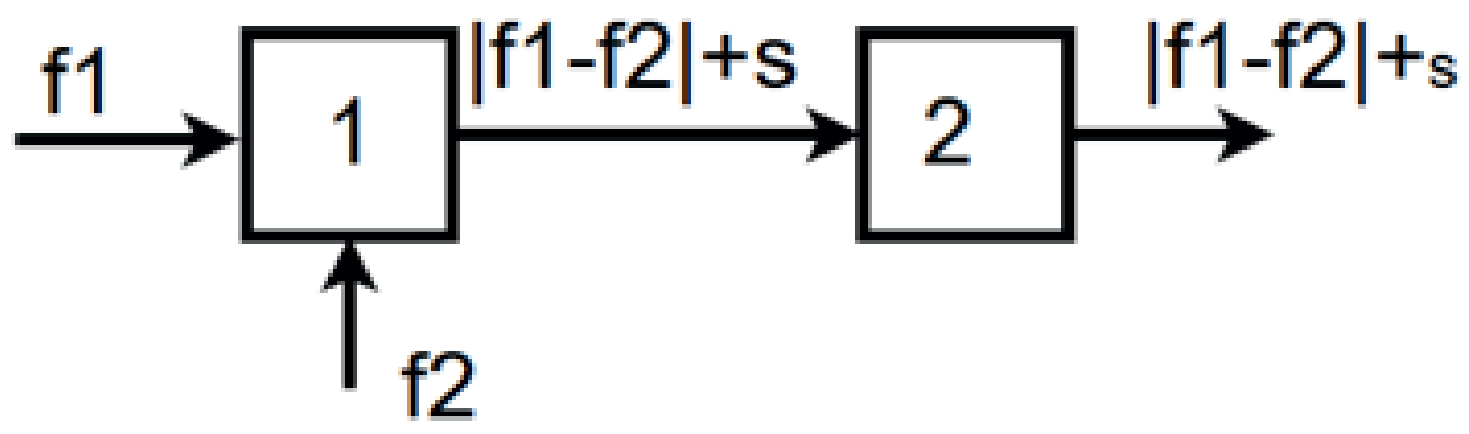
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### 1. INTRODUCTION



1: Digital mixer  
2: PLL based pass band filter  
F1, f2: square wave inputs signals  
S: spurs  
s: attenuated sp

Fig. 1 Functional diagram of the proposed mixer

Digital mixer:  
- Use digital circuits (digital gates)  
- Digital signals

### 2. MIXER DESIGN

- Analogue mixer can be expressed
- Replace analogue signal by digital
- Multiplication is XOR
- Implement addition
- Implement phase shift - (using Dflip)

#### Addition

A	B	A+B
-1	-1	-2
-1	1	0
1	-1	0
1	1	+2

- A and B are two level signal while A+B are three level signal,
- The first line is low level and is neither A NOR B, while the last one is high level and can be implemented as AND
- The output of the first line and last line will be input of RS trigger

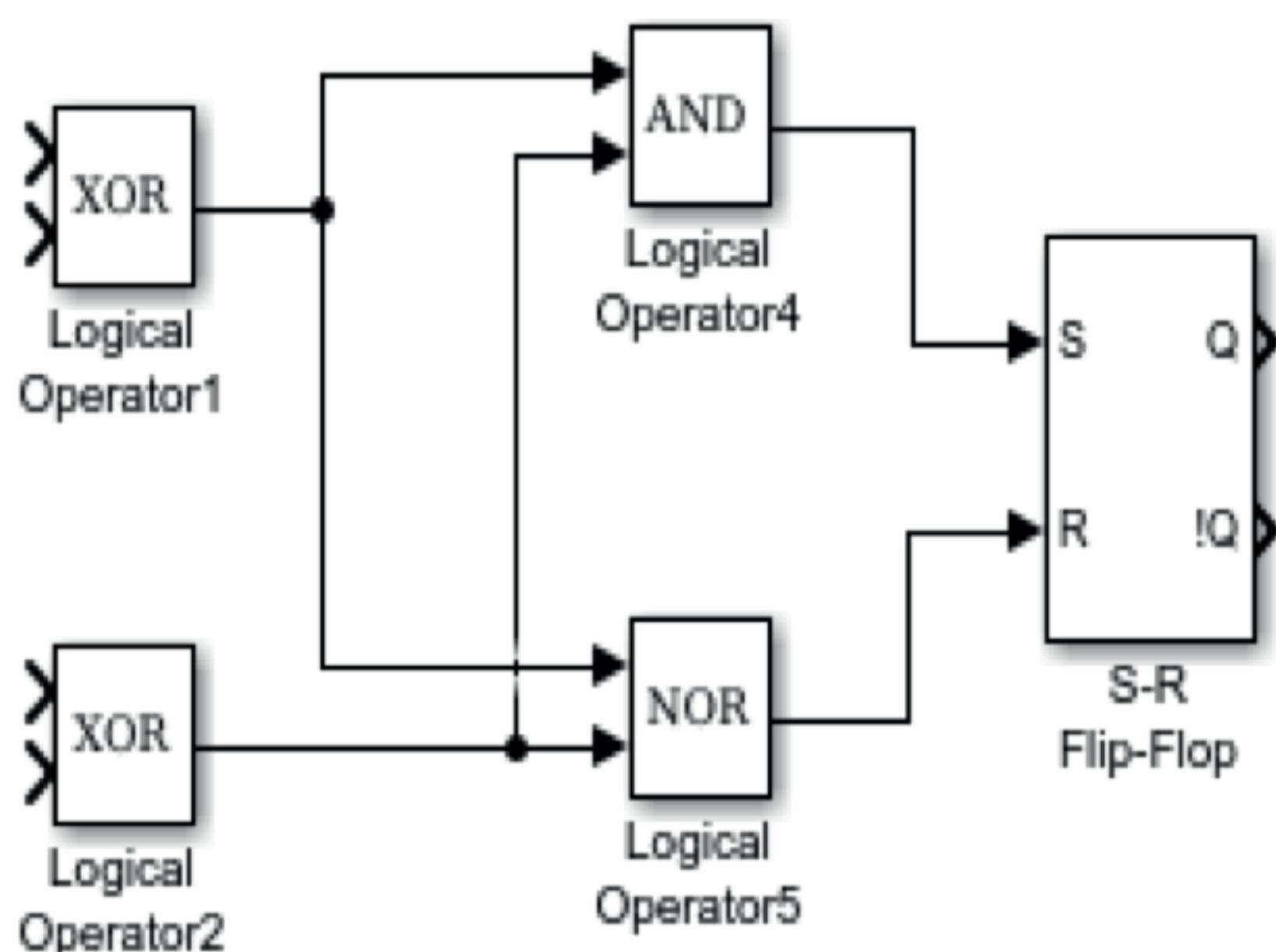


Figure 2. Digital mixer with digital logic

### 3. SIMULATION

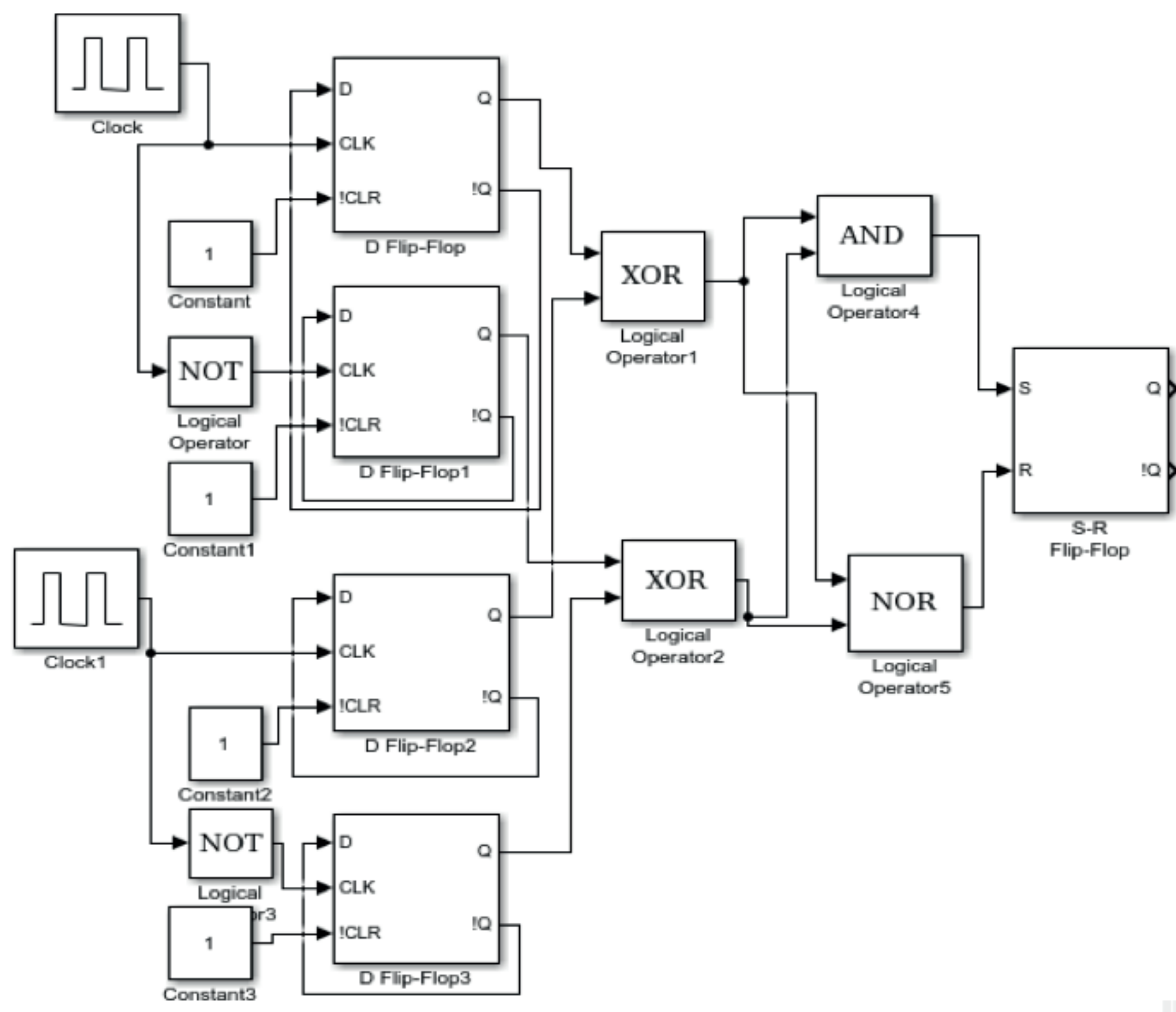


Figure 3: Simulation model using Simulink.

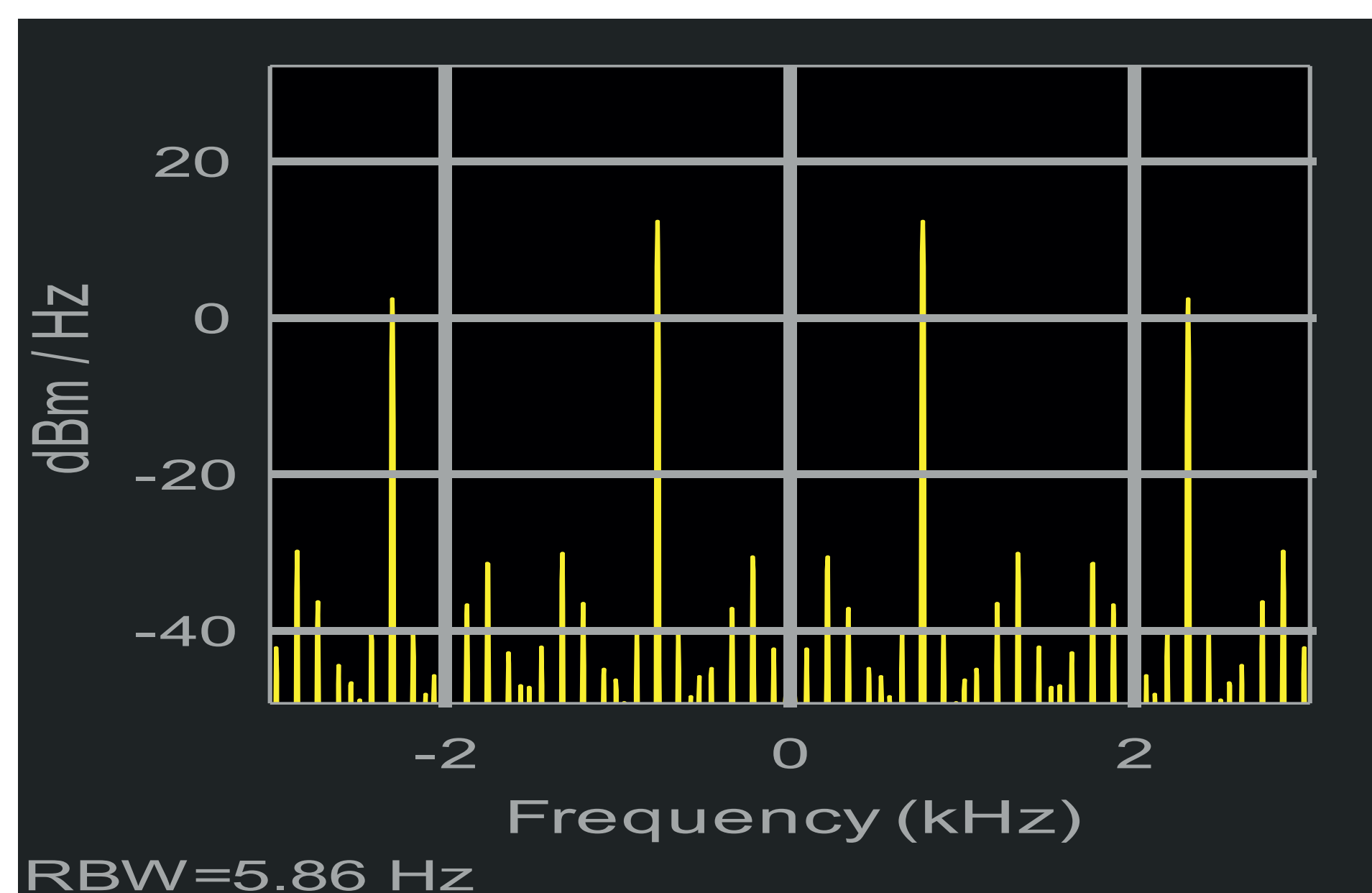


Figure 4. Output power spectrum f1=1530 Hz, f2=3060 Hz, fout=765 Hz.

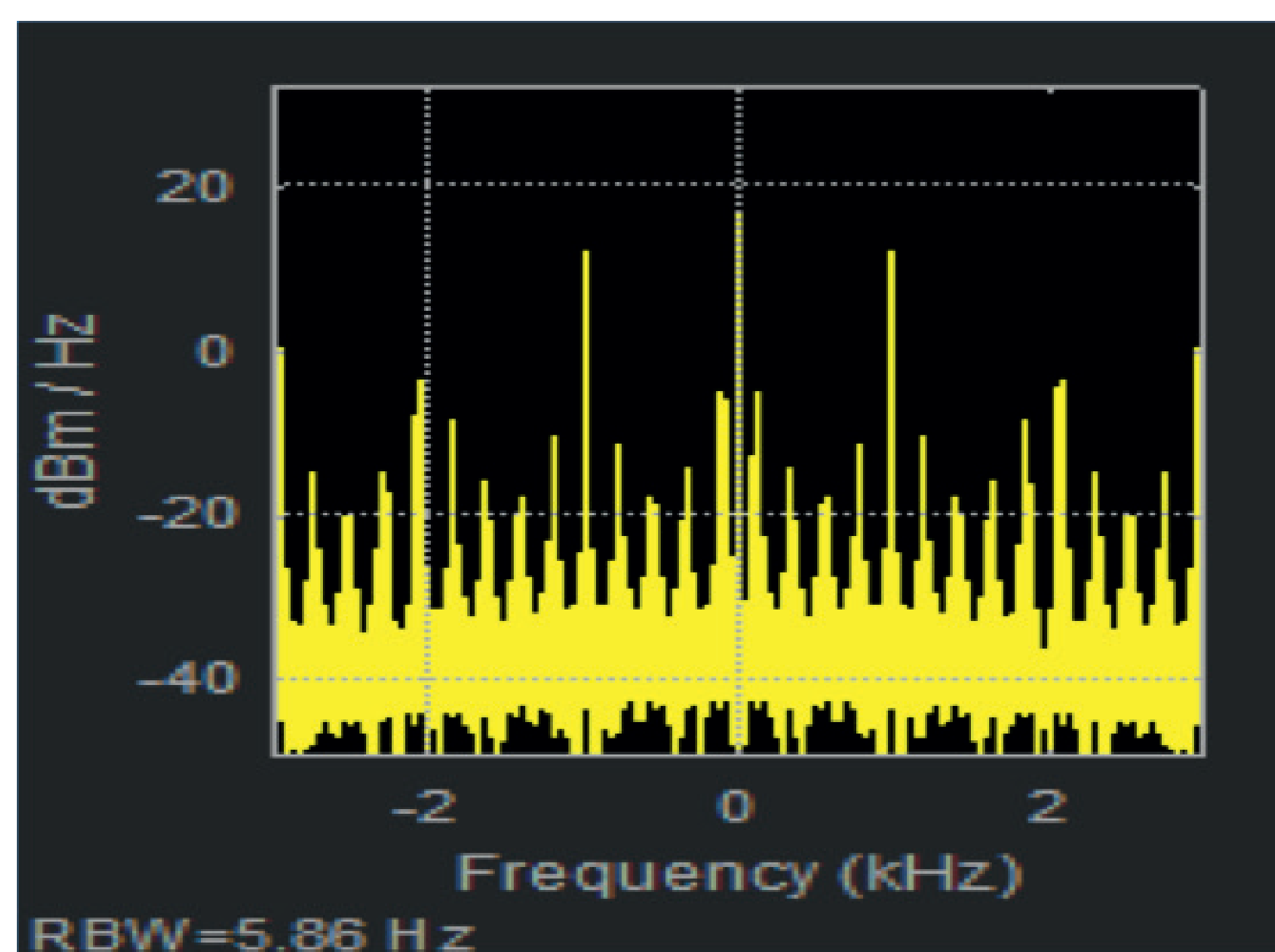


Figure 5. Output power spectrum f1=1530 Hz, f2=3500 Hz, fout=985 Hz.

### 4. IMPLEMENTATION AND MEASUREMENT

D flip flop CD74HC74E, NOT gate CD74HC04E, XOR gate CD74HC86E, NOR gate CD74HC02E, AND gate CD74HC08EE4, PLL chip CD74HC4046AE

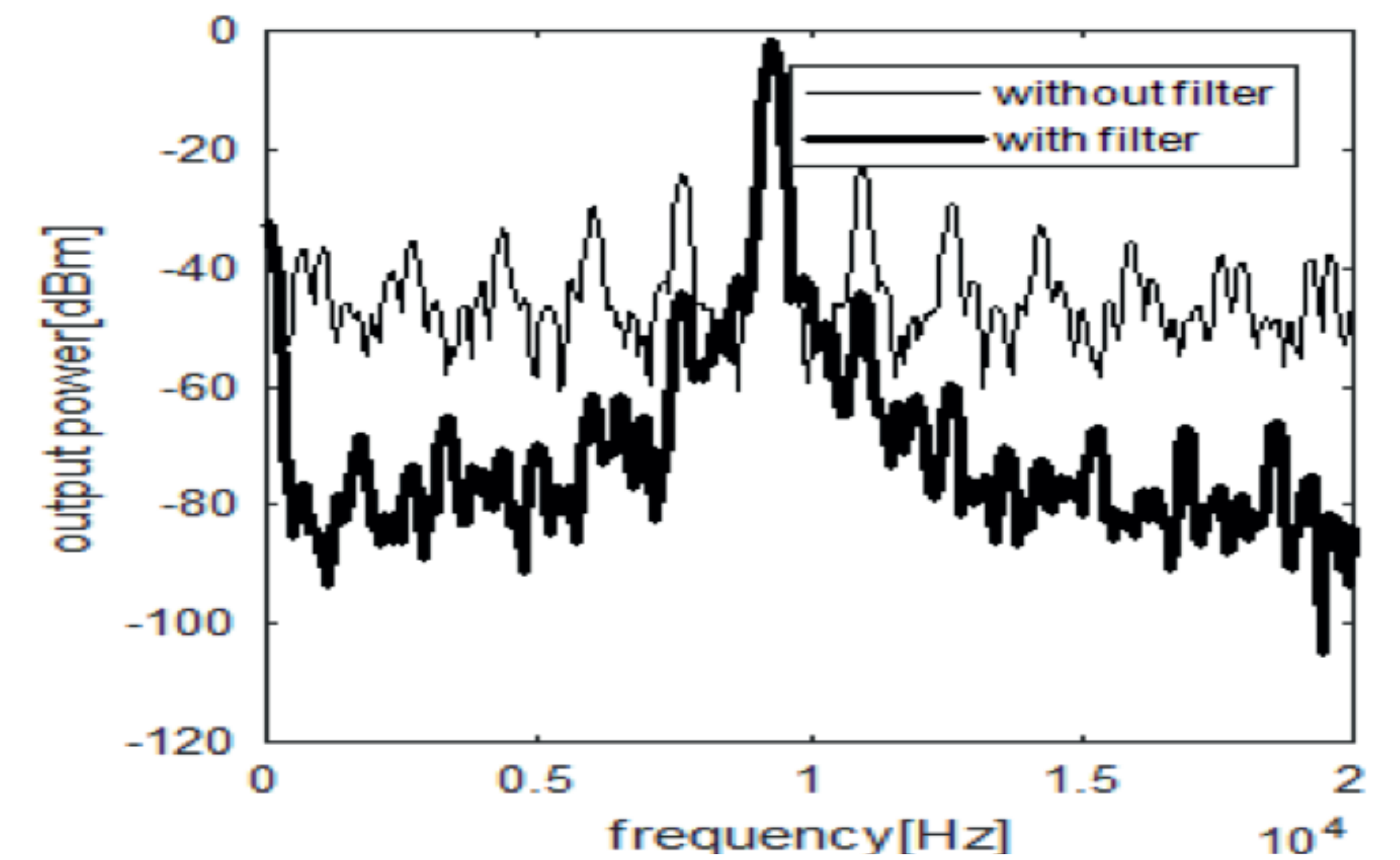


Figure 6. Output power spectrum with and without filter f1=56464 Hz, f2=37918 Hz, fout=9273 Hz.

### CONCLUSION

The digital mixer is realizable but has spurs, Careful filtering is needed

### REFERENCES

- [1] Ling W A and Sotiriadis P P A 2011 Nearly All-Digital Frequency Mixer Based on Nonlinear Digital-to-Analog Conversion and Intermodulation Cancellation IEEE transactions on circuits and systems Vol.58 NO.8 p. 1695-704
- [2] Cardells F and Valls J 2002 High Performance Quadrature Digital Mixers for FPGA" FPL2002 Montpellier France

